Notice of Allowability	Application No.	Applicant(s)	
	10/777,992	BRAUN ET AL.	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an examiners initiated interview and resulting amended claims dated 7/26/06*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Gero McClellan on 7/26/06, whereby:

Claims 1, 11, 15 and 17 are amended; and

Claims 2-10, 12-14, 16, 18-20 remain as originally presented.

3. The application's claims 1, 11, 15 and 17 are amended as follows:

1. (Currently Amended) A method for allocating memory arrangement addresses to a buffer chip, during an initialization mode, for use in addressing one or more memory arrangements connected to the buffer chip, comprising:

receiving first initialization data specifying a first set of available memory arrangement addresses;

associating one or more of the first set of available memory arrangement addresses with the one or more memory arrangements connected to the buffer chip;

generating, by the buffer chip, second initialization data specifying a second set of available memory arrangement addresses comprising the first set of available memory arrangement addresses less the memory arrangement addresses associated with the one or more memory arrangements connected with the buffer chip; and

transmitting the second initialization data from the buffer chip.

11. (Currently Amended) A buffer chip for use with one or more memory arrangements, comprising:

a reception unit for receiving first initialization data which specify available memory arrangement addresses;

~~a transmission unit for transmitting second initialization data; and~~

an initialization unit for, during an initialization mode, associating memory arrangement addresses with the one or more memory arrangements associated with the buffer chip, the associated memory arrangement addresses being chosen from the available memory arrangement addresses, wherein the initialization unit generates second initialization data specifying the memory arrangement addresses which are still available after the association, wherein the memory arrangement addresses which are still available after the association are those addresses specified in the first initialization data less the addresses associated with the one or more memory arrangements; and

a transmission unit for transmitting the second initialization data to another buffer chip.

15. (Currently Amended) A memory module, comprising:

one or more memory arrangements; and

a buffer chip coupled with one or more memory arrangements, wherein the buffer chip comprises:

a reception unit for receiving first initialization data which specify available memory arrangement addresses[[,]];

an initialization unit for, during an initialization mode, associating one or more of the available memory arrangement addresses with the one or more memory arrangements and generating second initialization data specifying the memory arrangement addresses which are still available after the association, wherein the memory arrangement addresses which are still available after the association are those addresses specified in the first initialization data less the

one or more addresses associated with the one or more memory arrangements; and

a transmission unit for transmitting the second initialization data.

17. (Original) A memory system, comprising:

a memory access control unit; and

one or more memory modules, each comprising one or more memory arrangements and a buffer chip coupled with one or more memory arrangements, wherein the buffer chip comprises:

a reception unit for receiving first initialization data which specify available memory arrangement addresses;[[,]]

an initialization unit for, during an initialization mode, associating one or more of the available memory arrangement addresses with the one or more memory arrangements and generating second initialization data specifying the memory arrangement addresses which are still available after the association, wherein the memory arrangement addresses which are still available after the association are those addresses specified in the first initialization data less the one or more addresses associated with the one or more memory arrangements; and

a transmission unit for transmitting the second initialization data.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PIERRE BATAILLE
PRIMARY EXAMINER
8/2/06